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Analysis of Leakages and Leakage Reduction Methods in UDSM CMOS VLSI Circuits.

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ABSTRACT
This is the era of portable devices which need to be powered by battery. Due to scarcity of space and leakages in chips, battery life is a serious concern. As technology advances, scaling of transistor feature size and supply voltage has improved the performance, increased the transistor density and reduced the power required by the chip. The maximum power consumed by the chip is the function of its technology along with its implementation. As technology is scaling down and CMOS circuits are supplied with lower supply voltages, the static power i.e. standby leakage current becomes very crucial. In Ultra Deep-submicron regime scaling has reduced the threshold voltage and that has led to increase in leakage current in sub-threshold region and hence rise in static power dissipation. This paper presents a critical analysis of leakages and leakage reduction techniques.

Keywords – leakage current, scaling, sub-threshold region, threshold voltage, UDSM.

I. INTRODUCTION

During the 90s, VLSI designers were focused primarily on improvising speed to work out crucially important real-time modules such as video alteration, games, graphics etc. This has resulted in Integrated circuits that have combined various complex signal processing blocks and graphics processing units to meet the office and entertainment requirements. While these efforts have solved the real-time problem, they leave the problem of increasing demand for portable operation unaccounted, where portable devices need to carry all this with consuming least possible power. The stern limitation on required power in portable electronics applications such as smart phones and tablets must be fulfilled by the VLSI chip designers while still keeping performance high. While wireless devices are a new buzz in the consumer electronics market, an important design constraint for portable operation is power consumption of the device. The key is - to improve life time with minimum requirements on dimensions, battery time and weight of the batteries. So the most central factor to consider while designing ICs for portable devices is 'low power design'.

This paper is organised as follows: section 1 deal with introduction and need for low power design. Section 2 deals with sources of power dissipation in CMOS gates. Section 3 deals with low power design. Section 4 deals with various low power design approaches. Conclusion and future work is given in section 5.

II. SOURCES OF POWER DISSIPATION

Power consumed by the ICs is divided as Dynamic, Short Circuit and Static. In submicron and later stages, static power reduction is the focus of design. Static power corresponds to various leakages at transistor level.

There are roughly six major leakage currents. Reverse bias junction leakage ($I1$) is from the source/drain into the substrate through the reverse biased diodes. Gate oxide tunnelling leakage ($I2$) is due to electron tunnelling from gate to substrate and vice versa due to thin oxide. Hot carrier injection ($I3$) is due to crossing of $Si\text{-}SiO_2$ interface potential barrier by electrons or holes. Gate Induced Drain Leakage ($I4$) is due to carrier production through avalanche multiplication and band - band tunnelling. Channel punch through current ($I5$) is due to merging of source-substrate and drain-substrate depletion regions due to short channel. The most important of these is Sub-threshold Leakage Current ($I6$). It is given by

$$I_{sub} = Io*e^{[V_{GS} - V_{TH}/nV_T]} [1 - e^{-V_{DS}/V_T}] \qquad ---- (1)$$

Where $Io = (\mu oCoxVT2e1.8(W/L))$, $VT = KT/q$ is the thermal voltage, VTH is the threshold voltage, VGS is the gate to source voltage, VDS is the drain to source voltage, W and L are the transistor width and length respectively. Cox is the gate oxide capacitance, μo is the carrier mobility and n is the sub threshold swing coefficient.

III. LOW POWER DESIGN

Low power design can be achieved at various abstraction levels. The methods at these abstraction levels are as given below.

At the system level, we have methods such as Partitioning and Power down. At Algorithmic level, we have Regularity, Complexity and Concurrency. At the architecture level, we can imply parallelism, data encoding, redundancy and pipelining. At the circuit level, we can reduce power by applying logic styles, transistor sizing and energy recovery. And at the technology level, we have multi threshold devices and threshold reduction for power reduction.

IV. VARIOUS LOW POWER DESIGN APPROACHES

There are various leakage reduction approaches or low power design approaches have been devised by the engineers. But each approach has some practical advantages as well as disadvantages. The basic parameters to be considered for the power reduction are mainly static leakage power, area and propagation delay. Some approaches combine two or more techniques which are compatible with each other to achieve more efficiency. These approaches are critically analyzed as follows.

1. Use of stacking

This approach is based on the fact that natural stacking of MOSFET helps in achieving less leakage current. The leakage through two series OFF transistor is much lower than that of single transistor because of stack effect. One such technique following this approach is Forced stack. In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It is a state retention technique but has backdrops as more dynamic power and area.

2. Use of sleep transistors

This approach uses the sleep transistor between both VDD and the pull up network and between GND and pull down network. The sleep transistor turn off the circuit by cutting off the power rails in idle mode thus can reduce leakage power effectively. In this technique we have floating values and thus will lose state during sleep mode. The Wakeup time and energy of the sleep technique have significant impact on the efficiency of the circuit. The techniques following this approach are Sleepy Keeper and Leakage feedback. Sleepy Keeper uses a PMOS transistor in parallel to NMOS sleep transistor in the pull down path and NMOS transistor in parallel to PMOS sleep transistor in the pull up path. The extra retention transistors are connected to the output so that during sleep mode the logic state is maintained, with high total power dissipation. But this technique increases dynamic power during active mode. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit.

Leakage feedback technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

3. Use of stacking along with sleep transistors

This approach combines the advantages of both sleep and stacking. The technique employing this approach is Sleepy stack. In this technique, one sleep transistor and two half sized transistors replaces each existing transistor. Although use of W/2 for the width of the sleep transistor is done, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitory circuit, for the sleep transistors.

4. Use of variable body biasing

This approach uses two parallel connected sleep transistors in Vdd and two parallel connected sleep transistors in GND. To reduce the leakage current in sleep mode we ensured that the body to source voltage of the sleep transistor is increased. The source of one of PMOS sleep transistor is connected to the body of other PMOS sleep transistor for having so called body biasing effect. Similarly the source of one of the NMOS sleep transistor is connected to the body of other NMOS sleep transistor for having the same effect as for PMOS sleep transistors. So, leakage reduction in this technique occurs in two ways. Firstly the sleep transistors effect and secondly, the variable body biasing effect. It is well known that PMOS transistors are not efficient at passing GND and NMOS transistors are not efficient at passing Vdd. But this variable body biasing technique uses PMOS transistor in GND and NMOS transistor in Vdd, both

are in paralleled to the sleep transistor, for maintain exact logic state during sleep mode.

5.   Use of various threshold levels

This approach is based on the fact that high Vth transistors are slow but have less leakage and low Vth transistors are fast but have high leakages. So, here appropriate combination of these is used as required. The techniques using this approach are given here. Dual-Vth assignment is one such technique. In this method, each cell in the standard cell library has two types as low Vth and high Vth. Gates with low Vth are fast but have high leakage, whereas gates with high Vth are slow but have less leakage. Conventional deterministic approaches for dual-threshold assignment utilize the timing slack of non-critical paths to assign high Vth to some or all gates on those non-critical paths to minimize the leakage power.

Another such technique is Multiple Vth CMOS. An MTCMOS circuit is implemented by inserting high Vth transistors between the power supply voltage and the original transistors of the circuit. The original transistors are assigned low Vth to enhance the performance while high-Vth transistors are used as sleep controllers. In active mode, SL is set low and sleep control high-Vth transistors are turned on. Their on-resistance is so small that VSSV and VDDV can be treated as almost being equal to the real power supply. In the standby mode, SL is set high and sleep control high-Vth transistors are turned off and the leakage current is low. The large leakage current in the low-Vth transistors is suppressed by the small leakage in the high-Vth transistors. By utilizing the sleep control high-Vth transistors, the requirements for high performance in active mode and low static power consumption in standby mode can both be satisfied.

SCCMOS technique is very much similar to the MTCMOS but instead of a high Vth sleep transistor, a nominal Vth sleep transistor is employed to reduce the additional delay caused due to the presence of increased threshold value in sleep transistor. Variable Threshold CMOS (VTCMOS) is a circuit design technique that has been developed to reduce standby leakage currents in low Vdd and low Vt applications. Rather than employing multiple threshold voltage process options, a VTCMOS circuit inherently uses low threshold voltage transistors, and the substrate bias voltages of the NMOS and PMOS transistors are generated by the variable substrate bias control circuit.

6.   Use of optimized input vectors

This approach follows the concept that sub-threshold leakage current depends on the vectors applied to the gate inputs because different vectors cause different transistors to be turned off. When a circuit is in the standby mode, one could carefully choose an input vector and let the total leakage in the whole circuit to be minimized model leakage current by means of linearized pseudo- Boolean functions.

7.   Use of zigzag technique

In this approach, sleep transistors are used in a zigzag or alternate manner with Vdd and GND. Wake-up cost can be reduced in zigzag technique but still state destruction is a limitation. Thus, any specific state which is needed on wakeup must be regenerated by any means. Thus the technique may need extra circuitry to generate a specific input vector.

8.   Use of GALEOR and LECTOR

In these two approaches, leakage control transistors are used to create stacking effect. In the LECTOR method two extra Leakage Control Transistors (a P-type and an N-type) are inserted within the gate, where the gate terminal of each Leakage Control Transistor is controlled by the source of the other. GALEOR technique reduces the leakage current flowing through the CMOS logic gate using stack effect where two drain controlled gated transistors are used. These two techniques are very good at leakage reduction but there is no provision of sleep mode of operation.

9.   Use of LPSR approach

The Low Power State Retention approach makes use of a pair of NMOS and PMOS transistors in the pull-up and pull-down paths of the CMOS circuit. The LPSR logic gate has four modes of operation as Active Mode, Deep Sleep Mode, State Retention Mode 1, and State Retention Mode 0. The LPSR approach has active mode static power less than other sleepy techniques and the least static power during deep sleep state and good state retention at low power. This approach has least total power dissipation during pulsed operation. Since only single Vt transistors are used in all the designs to achieve ultra low power operation, the novel technique provides new choice to the designers of low power VLSI circuits.

V. CONCLUSION

Out of the above mentioned approaches, GALEOR, LECTOR and LPSR approaches are used quiet widely in the ultra deep submicron regime(<100nm). These approaches are very efficient in terms of reducing static leakage power consumption. But they also suffer some compromises.

In future an improvement of them or combination of these approaches with some other

techniques to remove their backdrops needs to be done. One such combination of GALEOR with sleep and state retention elements is under study.

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